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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,111	12/15/2003	Dong Wei	200313534-2	5499

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EXAMINER	
MEHRMANESH, ELMIRA	
ART UNIT	PAPER NUMBER
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/737,111	WEI, DONG	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The application of Wei, for a "Method and apparatus for providing updated processor polling information" filed December 15, 2003, has been examined.

Claims 1-20 are presented for examination.

Claims 1, and 3-20 are rejected under 35 USC § 102.

Claim 2 is rejected under 35 USC § 103.

Claim Objections

Claims 16 and 19 are objected to because of the following informalities: "updator" needs to be changed to "updater" on lines 11, and 14 of claim 16 and line 3 of claim 19. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, and 3-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Takashima et al. (U.S. Patent No. 6,347,372).

As per claim 1, Takashima discloses a method for providing updated processor polling information (Fig. 4) comprising:

collecting processor polling information at boot time to be provided to an operating system, said processor polling information describing operating conditions of an integrated processing system (Fig. 4, element 36)

notifying the operating system that a triggering event has occurred, wherein said triggering event potentially alters said operating conditions of said integrated processor system (col. 8, lines 2-9)

providing updated processor polling information during runtime to said operating system (col. 7, lines 43-46) said updated processor polling information reflecting operating conditions of said integrated processor system after the occurrence of the triggering event (col. 7, lines 26-42).

As per claim 3, Takashima discloses the triggering event is based on an addition of a processor device (Fig. 8).

As per claim 4, Takashima discloses the triggering event is based on a deletion of a processor device (Fig. 8).

As per claim 5, Takashima discloses the triggering event is based on a deconfiguration of a processor device (col. 15, lines 6-13).

As per claim 6, Takashima discloses performing a process on an object associated with a processor device and returning a value to an operating system of said

integrated processor system, wherein said value supercedes a corresponding processor polling information (col. 10, lines 4-22).

As per claim 7, Takashima discloses the value that is returned is a zero indicating that the corresponding processor device is not to be polled (col. 10, lines 22-25).

As per claim 8, Takashima discloses the value that is returned is a non-zero number indicating a minimum polling frequency (col. 10, lines 4-25).

Claims 9-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Schultz et al. (U.S. Patent No. 6,948,094).

As per claim 9, Schultz discloses a computer program embodied on a computer readable medium (col. 2, lines 25-28) for providing updated processors polling information (col. 13, lines 36-46), the computer program causing a computer to perform the steps of:

creating a processor polling information table, said processor polling information table being populated with boot time processor polling information, wherein said processor polling information describes operating conditions of an integrated processing system (col. 13, lines 36-46)

updating said processor polling information table upon receipt of a notification that a triggering event has occurred, wherein said triggering event may potentially alter said operating conditions of said integrated processor system (col. 15, lines 29-35).

As per claim 10, Schultz discloses said computer program further causes said computer to:

invoke a bus check notification (col. 9, lines 66-67 through col. 10, lines 1-3) upon an online addition of a processor device, wherein said bus check notification indicates to an operating system that a re-enumeration of a device tree needs to be performed, and wherein said operating system invokes a Poll for corrected Platform Error (_PPE) procedure that returns a value indicating a polling frequency for said added processor device (col. 13, lines 36-46).

As per claim 11, Schultz discloses said computer program further causes a computer to: invoke an eject request notification upon an online deletion of a processor device, wherein said eject request notification indicates to an operating system to update its CPEP table and not poll from said processor device which has been deleted (col. 17, lines 27-41).

As per claim 12, Schultz discloses said computer program further causes a computer to: invoke a CPEP check notification invoked by an online deconfiguration of a faulty processor device, wherein the CPEP check notification indicates to an operating

system to invoke a _PPE procedure indicating to said operating system alternative processor devices to be polled (col. 17, lines 27-41).

As per claim 13, Schultz discloses said computer program further causes a computer to: invoke a _PPE procedure object associated with a processor device, wherein said _PPE procedure object returns a value that supercedes a corresponding CPEP table processor polling information (col. 17, lines 27-41) and (col. 13, lines 36-46).

As per claim 14, Schultz discloses a zero return value indicates that said corresponding processor is not to be polled (col. 13, lines 36-46).

As per claim 15, Schultz discloses a non-zero return value indicates a minimum polling frequency (col. 13, lines 36-46).

As per claim 16, Schultz discloses an apparatus for updating processor polling information (col. 15, lines 29-35) comprising:

a corrected platform error polling (CPEP) table creator for creating a CPEP table coupled to an operating system, said CPEP table being populated with boot time processor polling information, wherein said processor polling information describes operating conditions of an integrated processor system (col. 13, lines 36-46)

a triggering event detector coupled to said operating system, said triggering event detector capable of detecting an occurrence of a triggering event, where said triggering event may potentially alter said operating conditions of said integrated processor system (Fig. 3)

a CPEP table updator coupled to said operating system and further coupled to said triggering event detector, wherein, upon a receipt of a notification of an occurrence of a triggering event from said triggering event detector, said CPEP table updator provides updated processor polling information to said operating system based on said altered operating conditions (col. 13, lines 36-46) and (col. 15, lines 29-35).

As per claim 17, Schultz discloses the triggering event detector is configured to detect an event triggered by an addition or deletion of a processor device (col. 17, lines 27-41).

As per claim 18, Schultz discloses the triggering event detector is further configured to detect an event based on a deconfiguration of a processor device (col. 17, lines 27-41).

As per claim 19, Schultz discloses a polling frequency calculator coupled to said CPEP table updator (col. 15, lines 29-35), said polling frequency calculator configured to return a value that indicates a minimum polling frequency for a selected processor

device (col. 13, lines 36-46).

As per claim 20, Schultz discloses said polling frequency calculator is configured to forgo polling said selected processor device when said polling frequency calculator returns a zero value for said selected processor device (col. 17, lines 27-41) and (col. 13, lines 36-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima et al. (U.S. Patent No. 6,347,372) in view of Schultz et al. (U.S. Patent No. 6,948,094).

As per claim 2, Takashima fails to explicitly disclose a corrected platform error.

Schultz teaches:

creating a corrected platform error polling (CPEP) table, wherein said CPEP table is populated with processor polling information collected at boot time (col. 13, lines 36-46).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of boot control device of Takashima et al. in combination with method of correcting a machine check error of Schultz et al. to effectively correct system errors.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Takashima et al. discloses polling processors to detect their status (col. 7, lines 26-30). He also discloses of an error detection unit detects whether an error occurs in the processor-status data output by the "N" processors of the processor block 31 (Fig. 4, element 37). Schultz et al. discloses system error handling and correction (Fig. 3).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Nguyen et al. (U.S. Patent No. 6,021,475), "Method and apparatus for polling and selecting any paired device in any drawer".

Mano (U.S. Patent No. 6,012,151), "Information processing apparatus and distributed processing control method".

Klecka et al. (U.S. Patent No. 6,393,582), "Error self-checking and recovery using lock-step processor pair architecture".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).